AN IMPROVED DC-LINK VOLTAGE FUZZY LOGIC CONTROL STRATEGY FOR GRID CONNECTED CONVERTERS

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Abstract—This thesis presents a robust control strategy to improve dc-link voltage control performances for Grid connected Converters (GcCs). The proposed control strategy is based on an fuzzy controller and is aimed to ensure fast transient response, low dc-link voltage fluctuations, low grid current THD and good disturbance rejection after sudden changes of the active power drawn by the GcC. The proportional and integral gains of the considered fuzzy controller are self-tuned so that they are well suited with regard to the operating point of the controlled system and/or its state. Several simulation and experimental results are presented to confirm and validate the effectiveness and feasibility of the proposed dc-link voltage control strategy.

Index Terms—DC-link voltage control, Fuzzy Controller, Grid connected Converters

INTRODUCTION

Nowadays, power converters have an important role in a large scale of industrial applications since they allow efficient power transmission between the grid (on one side) and loads or energy sources (on the other side). The commonly used power converters topologies use a dc-link as an intermediate stage for the power conversion process in addition to a Grid connected Converter (GcC) and a filter based on passive (inductive and/or capacitive) elements. For example, this is the case of adjustable speed drives [1-2], renewable energy sources [3-4], active power filters [5-6], UPS systems [7] and back-to-back systems [2],[8]. Efficient dc-link voltage control is very important for such applications to reduce voltage fluctuations in the dc-link [9], which are mainly caused by random changes (particularly sudden and sever changes) in the power drawn by the GcC. When these fluctuations cross their limits, the protection devices are activated leading to a system shut-down [3],[9]. Thus, the control objectives pertaining to the dc-link voltage can be summarized in the following key points: 1) the voltage across the dc-link capacitor must be kept at a constant value by controlling the power flow in the AC side of the GcC so that two objectives are satisfied: the first one is the upkeep of the capacitor charge, while the second one is the supply of a load connected to the dc-link (for the rectifying mode case) or the transfer of the power provided by a DC source (for the inverting mode case), 2) the dc-link voltage fluctuations must be minimized, 3) the generation of high grid current harmonics must be prevented and 4) The deviation from the unity power factor operation caused by the grid current ripples must be prevented. The most frequently used dc-link voltage controller is the PI controller [10],[11]. Different PI controller design techniques were described in literature. Among them, we can cite the pole zero cancellation method, the pole placement method and the optimum criterion method [8],[11]. For these methods, the PI controller is usually adjusted with respect to different constraints: C1) stability; C2) dynamic performances; C3) disturbance rejection; and C4) step responses with low overshoot [12]. In order to satisfy all these constraints, some research works presented the design of adaptive PI controllers [13-17]. Other ones combine between the benefits of the PI controller and the feed forward compensation method [18-20]. For that case, despite the excellent improvement of dynamic performances, such a method increases the coupling between the controlled dc-link voltage and the grid currents. Consequently, any noise or fast oscillation in the grid currents can create ripples at the output reference of the dc-link voltage controller. Other works have presented a Direct Power Control (DPC) combined with the boundary control [26] to improve the dynamic performances of the dc-link voltage. Compared to the conventional DPC, the dc-link voltage is considered for selection of the switching states through a switching table. As a result, no outer loop is needed and the dynamic performances are highly improved. However, this method results into a
variable switching frequency, which is limited to the half of the used sampling period and which depends on the system parameters, dc-link voltage and ac-side voltage [23], [27]. So, the DPC combined with boundary control cannot be used for applications that require constant switching frequency, like the case of LCL-based GcCs since it will lead to resonance problems. Moreover, this control will lead to high grid current THD values during steady state operation if low mean switching frequency is achieved.

II. DC-DC CONVERTERS

A DC-DC converter with a high step-up voltage, which can be used in various applications like automobile headlights, fuel cell energy conversion systems, solar-cell energy conversion systems and battery backup systems for uninterruptible power supplies. Theoretically, a dc-dc boost converter can attain a high step-up voltage with a high effective duty ratio. But, in practical, the step-up voltage gain is restricted by the effect of power switches and the equivalent series resistance (ESR) of inductors and capacitors.

Generally a conventional boost converter is used to get a high-step-up voltage gain with a large duty ratio. But, the efficiency and the voltage gain are restricted due to the losses of power switches and diodes, the equivalent series resistance of inductors and capacitors and the reverse recovery problem of diodes. Due to the leakage inductance of the transformer, high voltage stress and power dissipation effected by the active switch of these converters. To reduce the Voltage spike, a resistor-capacitor –diode snubbed can be employed to limit the voltage stress on the active switch. But, these results in reduction of efficiency. Based on the coupled inductor; converters with low input ripple current are developed. The low input current ripple of these converters is realized by using an additional LC circuit with a coupled inductor.

III. PROJECT DISCRIPTION

A. Modeling and design of the dc-link voltage controller

The studied system is depicted on Fig.1.a, where L (respectively R) is the filter inductor (respectively the filter resistor); C is the capacitor of the dc-link; \( V_g(a,b,c) \) refer to the components of the grid voltage vector in the natural reference frame; \( i_g(a,b,c) \) refer to the components of the grid current vector in the natural reference frame; \( S(a,b,c) \) are the GaC switching states; \( V_{dc} \) is the dc-link voltage; \( V_{dc}^* \) is the dc-link voltage reference; \( idc \) is the current coming out from the power converter; \( ic \) is the current flowing into the capacitor \( C \); \( i \) is the current consumed/generated by the load/the DC source connected to the dc-link; and \( ig(d,q) \) are the d and q components of the grid current reference in the synchronous reference frame \( (d,q) \), where the d axis is linked to the grid voltage vector. Fig.1.a shows also that the control structure of a GcC includes three main functions: the grid synchronization [21], the current controller [22] and the dc-link voltage controller [11]. Fig.1.b shows the model of the dc-link voltage control system. In this figure, GS and CC stand for grid synchronization and current controller, respectively. It can be noted that the dc-link voltage control is not in the form of a LTI system. This is mainly due to nonlinearities introduced by the idc table that computes idc current based on grid currents \( ig(a,b,c) \) and applied switching signals \( S(a,b,c) \). To simplify the model, the relationship between the mean value of idc (idc mean) and \( ig \) * currents is firstly determined. This relationship is deduced according to equation (1) [20]. In this equation, PAC is the active power fed in the AC side of the GcC, \( V_{gm} \) is the magnitude of the phase voltage, \( ig \) is the d component of the grid current and PDC is the active power fed in the DC side of the GcC. Supposing that \( V_{dc}=V_{dc}^* \) and neglecting the power losses on the GcC and on the internal resistor of the inductive filter (PAC=PDC), the relationship between idc mean and \( ig \) * currents can be deduced as shown in equation. For a simplest, but reasonably accurate modeling of the dc-link voltage control, the simplified model given by Fig.1.c is considered. This simplified model is based the following assumptions: 1) the dynamic of CC loop is very fast with regard to that of the dc-link voltage control loop and 2) the nonlinearities are neglected. According to Fig.1.c, the dc-link voltage controller has two inputs: 1) the dc-link voltage reference \( V_{dc}^* \) and 2) the input current \( i \). To study the dc-link voltage control loop, the superposition method is considered. Using this method and supposing that the PI controller transfer function is equal to \( (K_{pdc}+K_{idc})/s \), two systems are derived from Fig.1.c. For the first system (Fig.1.d and equation (2)), \( i \) is neglected, while \( V_{dc}^* \) is
considered as an input. For the second system (Fig.1.e and equation (3)), i is considered as an input, while Vdc * Identifying denominators of (2) and (3), we deduce that 2ξω=FKpdc/C and on 2 =FKidc/C, where ξ is the damping ratio and on is the natural frequency of oscillation. The poles p(1,2) of the transfer functions given by (2) and (3) are equal to -ξω=1+jω=1-ξ2 ) for 0≤ξ≤1. So, the system stability is guarantee whenever (4) is verified.

Analysis of the grid current harmonics

To derive the relationship between the output current harmonics and the selected (ξ,ωn) values, it shall be noticed that the grid current harmonics are affected by the ripples that may exist in the dc-link voltage controller output signal. These ripples are the result of the oscillating nature of the idc current. To simplify the study, let consider the case when the GcC operates with a constant switching frequency fc. For that case, and according to [28], the dc-link current can be expressed according to equation (10). Where Φ1, Φωc 1 and Φωc 2 are constant phase angles, m is the modulation index, ωc=2πf=2π50 rad/s is the frequency of the grid currents, oc=2πfc is the switching frequency, Igm is the grid current magnitude, Ioc and I2ωc are the magnitudes of the main harmonic components (i.e. for the frequencies equal to oce=3ω and 2ωc , respectively). Note that Ioc and I2ωc are proportional to the grid current magnitude Ig with a coefficient that depends on the used modulation index m [28]. The pulsating current idc passes through the 1/(Cs) bloc to create the bus-voltage ripples. Given that Ioc and I2ωc are proportional to the grid current magnitude Ig with a coefficient that depends on the applied modulation index m [28], the NCCR depends on the used capacitor, the used switching frequency, the used modulation index m and the selected gains Kpdc and Kide for the PI controller. The ripples around the switching frequency in the dq synchronous reference frame (i.e. respectively (fc-3f), (fc-3f) and 2fc) become respectively (fc-2f), (fc-2f) and (2fc+f) ripples in the natural reference frame. Assuming that Hcc(s) is the closed-loop transfer function of the internal current control loop, the grid current will have harmonic content with a magnitude equal to NCCR1×|Hcc(jωc)|+NCCR2×|Hcc(j(ωc+4ω))|+NCCR3×|Hcc(j(2ωc+ω))|. This harmonic content will influence the grid current THD especially for low dc bus capacitor values, low switching frequency values and high selected Kpdc and Kide gains (when on increases). For the case of variable switching frequency, it is difficult to derive the main harmonic content of the dc-link voltage. However, for a given main harmonic content, the grid current THD is influenced in the same manner as the case of a constant switching frequency operation.

3.1 PROPOSED ADAPTIVE PI CONTROLLER

A. Design of the adaptive PI controller

The discrete-time model of the proposed adaptive PI controller is given by equation (14). In this equation, the proportional and integral gains (Kpdc, Kpdc) are determined using an adaptive process, which is aimed to minimize the dc-link voltage transients (i.e. during transient states) and the grid current THD (i.e. during steady states). To avoid large overshoots of the bus voltage, especially after step jumps of the dc-link voltage reference Vdc *, an anti-windup correction [24] was added.

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The values of the higher and lower band limits are equal to $V_{dc}^* + G_{dc} V_{dc}^*$ and $V_{dc}^* - G_{dc} V_{dc}^*$, respectively. Outside the band, especially during startup or after step changes of the dc-link voltage reference $V_{dc}^*$, the natural frequency $\omega_n$ is selected equal to $\omega_{n_{max}}$. In this case, the controller is employed as a standard PI with an anti-windup action. Inside the band, the $\omega_n$ value depends on the magnitude of the dc-link voltage error $|\Delta V_{dc}|$ and is selected according to the function given by equation (15). The main purpose of this function is to increase the selected $\omega_n$ value when the magnitude of the dc-link voltage error $|\Delta V_{dc}|$ increases during transient states. Conversely, during steady states, when $|\Delta V_{dc}|$ is close zero, the selected $\omega_n$ value must be approximately equal to $\omega_{n_{min}}$ to lead to a low grid current THD.

The tuning of the adaptive PI parameters is detailed in the following:

1. How to set the parameter $G_{dc}$?
   - The voltage rating of the dc-link voltage capacitor and GeC power switches is computed under dynamic conditions with an appropriate safety factor. In general, 10% overshoot of the dc-link voltage is considered under dynamic conditions. To this purpose, the $G_{dc}$ gain (defined as the half of the ratio between the band value and $V_{dc}^*$) is chosen so that the dc-link voltage fluctuations remain lower than 10% $V_{dc}^*$, even after sudden and severe changes of the input current $i$. This means that, after a step jump of the input current $i$ equal to its maximum value $\pm I_{max}$, the dc-link voltage $V_{dc}$ must remain inside the band $\pm G_{dc} V_{dc}^*$ around the dc-link voltage reference $V_{dc}^*$. - How to set the parameter $G_{dc}$?

2. How to set the parameter $\omega_{n_{max}}$?
   - As mentioned previously, the dynamic of the CC loop is assumed very fast with regard to that of the dc-link voltage control loop. The time constant $\tau_v$ of the dc-link voltage control loop is equal to $1/Re(p(1,2))=1/\left(\xi \omega_n\right)$. Assuming that $\tau_i$ is the time constant of the CC loop, the time constant $\tau_v$ must be greater than $10 \tau_i$. In this work, the time constant of the used CC loop $\tau_i$ is lower than 1 ms. In order to achieve a time constant $\tau_v$ greater than 10 ms, the $\omega_{n_{max}}$ value must be lower than a maximum value $\omega_{n_{max}}$ equal to $1/(\xi*10 \tau_i)$. So, the $\omega_{n_{max}}$ value is selected equal to $142.86 \text{ rad/s}=2\pi 22.73 \text{ rad/s}$. - How to set the parameter $\omega_{n_{min}}$?
   - The $\omega_{n_{min}}$ value can be determined so that the response time $\tau_r$ (given by equation (9)) do not exceed a tolerable limit, even after maximum power load connection/disconnection. In this work the tolerable limit of $\tau_r$ is set 10 times the grid period ($\tau_r=10*20\text{ms}=200\text{ms}$). For a $\xi$ value set to 0.7 and based on equation (9), $\omega_{n_{opt}}$ is equal to $21.99 \text{ rad/s}=2\pi 3.5 \text{ rad/s}$. - How to set the parameter $\lambda$?

3. How to set the parameter $\lambda$?
   - The choice of the $\lambda$ value must take into account the following points: 1) For lower $\lambda$ values (close to zero), when the dc-link voltage error $|\Delta V_{dc}|$ increases, the selected $\omega_n$ value increases faster and shorter transient time can be achieved; 2) For higher $\lambda$ values (close to 1), smoother $\omega_n$ selected value is obtained during steady state operation. In this paper, the $\lambda$ value was set to 1 in order to select $\omega_n$ value approximately equal to $\omega_{n_{min}}$ during steady state operation to reduce grid current THD.

Simulation results

Simulations are done in order to compare the performances of the adaptive PI controller (including the anti-wind-up action) with those of the standard PI controller. The used simulation parameters are depicted on Tab.1 and the obtained simulation results are shown on Fig.3. Fig.3.a compares between simulations results obtained with the standard PI control (for constant PI gains tuned for $\omega_n=\omega_{n_{min}}$ and $\omega_n=\omega_{n_{opt}}$) and those obtained with the proposed adaptive PI control. The natural frequency $\omega_{n_{opt}}$ is determined so that, when a step jump equal to $I_{max}$ is applied to the input current $i$, the resulting $M_p$ value is equal to $G_{dc} V_{dc}^* =10\% V_{dc}^*$. So, based on equation (9), $\omega_{n_{opt}}$ is computed as follows:

$$\omega_{n_{opt}} = \frac{\max 5 * 416.88}{34.74 \text{rad/s} 0.1*150 \text{ nopt}} = 1.25 (0.7)$$

It can be noted that the adaptive PI control ensures shorter transient time with lower drop of the dc-link voltage.
voltage after a step jump (at t=0.5s) of the input current i equal to Imax.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>value</th>
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<tbody>
<tr>
<td>S</td>
<td>Ge.C rated power</td>
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<td>kVA</td>
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<tr>
<td>L</td>
<td>Inductive filter</td>
<td>40</td>
<td>mH</td>
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<tr>
<td>C</td>
<td>DC-link voltage capacitor</td>
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<td>μF</td>
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<td>Zload</td>
<td>Load Impedance</td>
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<td>Ω</td>
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<tr>
<td>Imax</td>
<td>Maximum load current</td>
<td>1.25</td>
<td>A</td>
</tr>
<tr>
<td>Vdc,ic</td>
<td>DC-link voltage initial value</td>
<td>100</td>
<td>V</td>
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<tr>
<td>Vdc,r</td>
<td>DC-link voltage reference value</td>
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<td>V</td>
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<td>Gv</td>
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<td>rad/s</td>
</tr>
<tr>
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<td>ωmax</td>
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<tr>
<td>ζ</td>
<td>Damping ratio</td>
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<tr>
<td>Kc</td>
<td>Anti-windup coefficient</td>
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<tr>
<td>Tc</td>
<td>Sampling period</td>
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IV. CONCLUSION
This paper presented an improved dc-link voltage controller based on an adaptive PI controller with an anti-windup process. The proportional and integral gains of the proposed PI controller are self-tuned so that the following constraints are satisfied: 1) no overshoot after step jumps of the dc-link voltage reference input; 2) fast dynamic response after step jumps of the dc-link voltage reference; 3) fast dynamic response after step jump of the input current i and 4) low grid current THD value during steady state operation. The considered control was experimentally tested on a prototyping platform. The obtained experimental results are quite similar to
simulation results and show the effectiveness and reliability of the adopted control strategy.

REFERENCES


[4] X. Yuan, F. Wang, D. Boroyevich, Y. Li, and R. Burgos, “Dc-link voltage control of a full power converter for wind generator operating (a) 5ms Vga 0dq 0 2π iga(THD=5.26%) Standard PI controller (ωn=ωopt) (b) 5ms Vga 0dq 0 2π iga(THD=4.12%) Proposed adaptive PI controller Vdc * iga ωn=ωmin 100ms Vdc t1=50ms tpic=100ms Mo=10V Vdc iga ωn=ωopt t1=33ms tpic=63ms Mo=10V Vdc * 100ms iga Adaptive PI Vdc Vdc * 100ms iga i (d) ωn=ωmin Vdc tp=51ms tr=200ms Mp=24V 100ms Vdc iga ωn=ωopt tp=32ms tr=127ms Mp=15V i 100ms iga Adaptive PI Vdc tp